

# Linear High-Efficiency Microwave Power Amplifiers Using Bandpass Delta-Sigma Modulators

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**Abstract**— A novel amplifier configuration is described, in which a bandpass delta-sigma modulator is used to produce a two-level (digital) signal representing an analog radio frequency (RF) input. Subsequently, a switching-mode amplifier and bandpass filter are used to amplify the signal and remove unwanted spectral components. This configuration has the potential of achieving high efficiency (typical of switching mode amplifiers) together with high linearity. A simulated implementation with GaAs heterojunction bipolar transistors (HBT) is shown.

## I. INTRODUCTION

THERE is significant interest in increasing the power-added efficiency (PAE) of microwave power amplifiers to address the needs of battery-operated communication systems. However, the most efficient microwave power amplifiers operate in a switching mode, or at best in a nonlinear class of operation [1], resulting in excessive spectral growth and loss of modulation accuracy for signals which have time-varying envelope. Such signals comprise many modulation formats currently in use, such as QPSK, OQPSK, etc. The desire to use high-efficiency switching mode amplifiers yet achieve high linearity has been the subject of various research efforts [2], [3]. In this letter we present a novel amplifier related to the Class *S* amplifier [3] employed for low-frequency signals, which is capable of producing output signals at frequencies in the microwave regime. The amplifier employs a bandpass delta-sigma modulator to encode the desired output signal into a binary level signal, which is subsequently fed into a switching-mode power amplifier. A bandpass filter is used to remove unwanted spectral components from the output. We show (by simulation) a potential implementation of the amplifier for operation at 800 MHz, utilizing GaAs heterojunction bipolar transistor (HBT) technology.

## II. AMPLIFIER CONFIGURATION

The proposed amplifier is shown schematically in Fig. 1. The incoming signal is taken to be an amplitude and phase-modulated radio frequency (RF) carrier centered around a known frequency (such as 800 MHz), band-limited such that its spectral components are within a well-established bandwidth range  $B$  (on the order of 25 MHz). The signal is passed through a bandpass delta-sigma modulator (BPDSM)

with 1-bit (two-level) output, and the resulting binary signal is fed into a switching mode amplifier. Finally, a bandpass filter is used at the amplifier output prior to the load. The output of the BPDSM is a binary signal, in which the quantization noise associated with the digitization is spectrally shaped so that it lies largely outside of the band of interest, in a manner determined by the order of the modulator and the characteristics of the resonator within it [4]. Practical implementation of this modulator circuit for handling 800-MHz RF signals has been reported recently [5] using GaAs HBT technology. In the following, we show SPICE simulations of the operation of the novel amplifier based on this reported modulator together with an HBT-based switching-mode amplifier (although the approach is more general). For an input sinusoid, Fig. 2 illustrates the waveforms in the time and frequency domains at different points in the bandpass class-*S* amplifier. The output spectrum shows the appropriate sinusoidal output, together with quantization noise, which is largely removed from the band of interest. The output spectrum also contains images of the input signal, at frequencies  $n \cdot f_{\text{clk}} \pm f_{\text{signal}}$ , where  $f_{\text{clk}}$  and  $f_{\text{signal}}$  are clock and signal frequencies, respectively, and  $n$  is an integer. After amplification in the switching mode amplifier, the signal undergoes bandpass filtering (within the amplifier output matching structure).

Fig. 3 schematically illustrates one of several possible implementations of the switching-mode amplifier for use in a NPN-only technology. In the configuration shown, the voltage across the transistor output terminals varies rapidly between a minimum value, near  $V_{\text{cesat}}$ , and the power supply voltage, near  $V_{\text{cc}}$ . Free-wheeling diodes provide the current flow during intervals when the transistors are off. To achieve high-efficiency it is necessary to minimize charge storage during transistor saturation (in the ON state). This can be achieved using double-heterojunction bipolar transistors (DHBT's) with wide bandgap collectors such as those reported in [6]. Fig. 4 illustrates the SPICE simulated voltage and current through the transistors and diodes for a representative design based on GaAs DHBT's ( $f_t, f_{\text{max}} = 55$  GHz). The output filter provides nonzero conductance essentially only in the band of interest, so there is no power dissipation associated with spectral components that do not reach the load.

## III. LINEARITY CONSIDERATIONS

Since the final switching (Class-*S*) stage can be regarded as a linear stage for the digital signal, the linearity of the amplifier is determined by the BPDSM. An ideal BPDSM is linear for input signals upto a level approximately 3 dB

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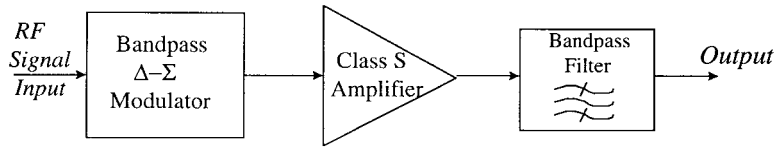


Fig. 1. Schematic structure of bandpass class- $S$  amplifier.

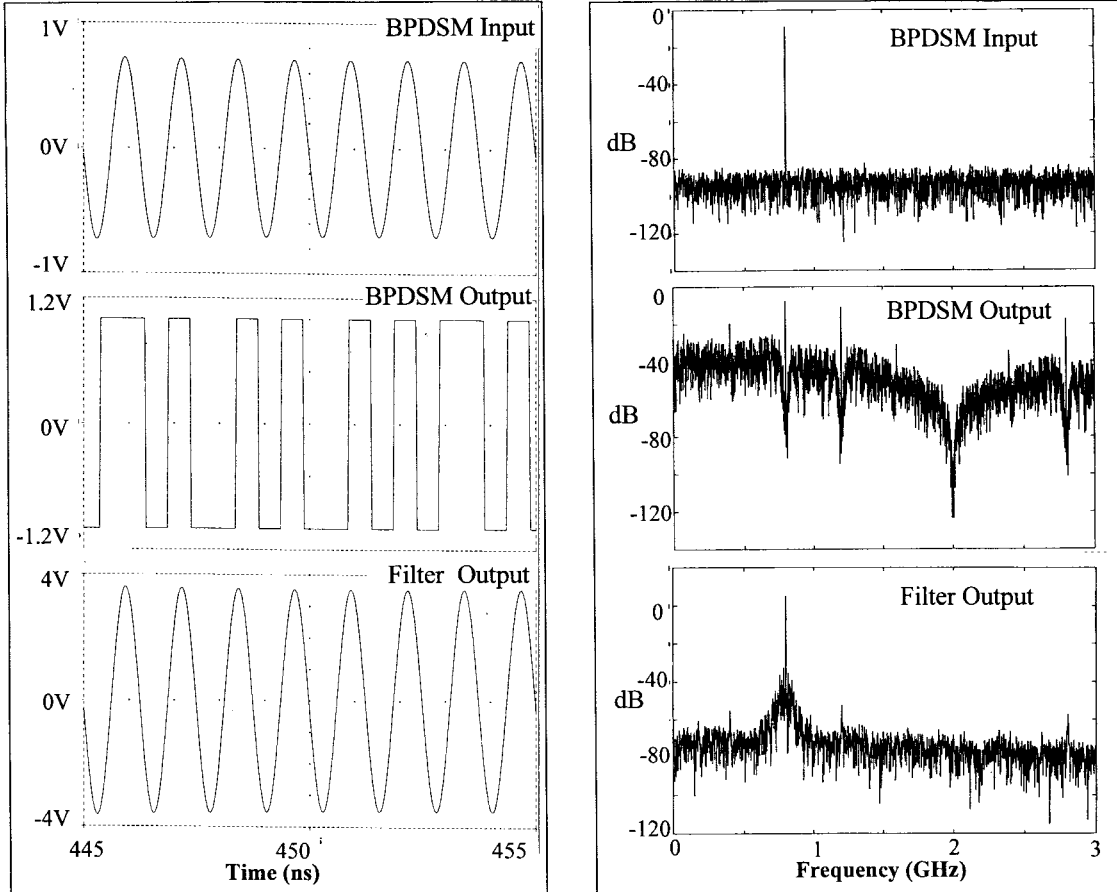


Fig. 2. Signals associated with the bandpass class- $S$  amplifier in time and frequency domain.

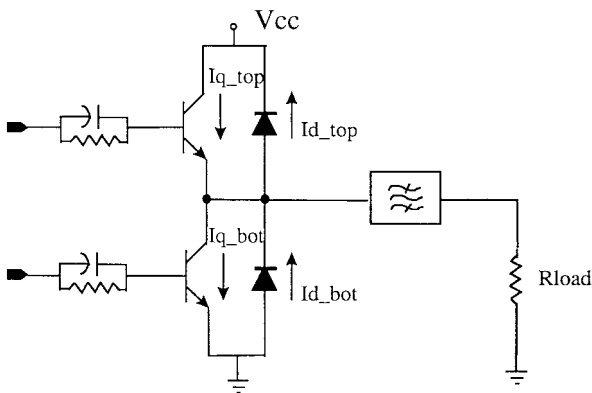


Fig. 3. NPN-only output amplifier.

below the step size  $\Delta$  of the quantizer. For signals below this level, in a practical implementation, the linearity of the input stage in the feedback loop sets the overall linearity of the system. Recently reported work [5] has demonstrated third-

order intermodulation products lower than  $-50$  dBc. Better linearity can be achieved with improved circuit designs. For signals above this level the nonlinearity of the quantizer can no longer be suppressed by the feedback, resulting in degradation of effective noise floor.

#### IV. PAE CONSIDERATIONS

The principal sources of power loss in the amplifier are:

- 1) power lost in the transistors during the ON-OFF transients;
- 2) energy associated with discharging parasitic capacitance associated with the output terminals of the transistors;
- 3) power needed to operate the BPDSM, and predriver for the output amplifier;
- 4) power lost in the transistors and diodes associated with their on voltage;
- 5) power lost in the passive elements, such as the output filter.

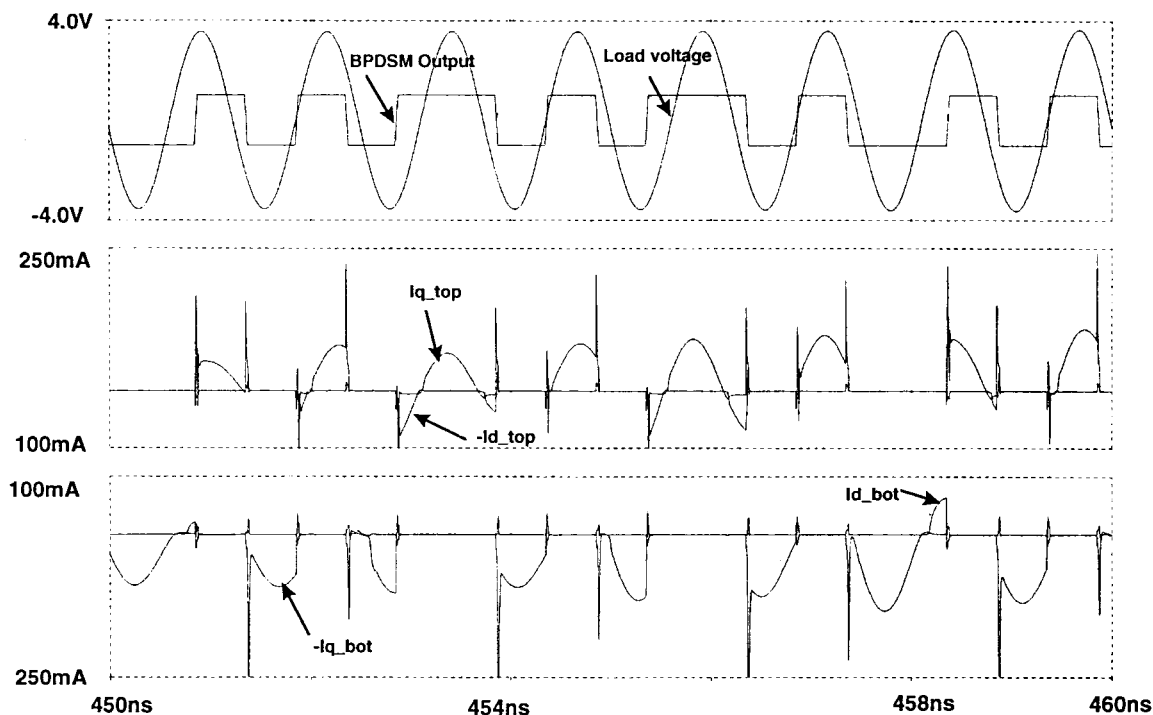


Fig. 4. Simulated voltage and current waveforms for the output stage of Fig. 4, implemented with GaAs HBT's and Schottky diodes.

The contributions listed as 1)–3) above increase as the rate of switching of the amplifier input increases, and thus require minimizing the clock frequency of the BPDSM. However, the output power that can be accommodated with a given amplifier and power supply voltage also varies with clock frequency as approximately  $[\sin(\pi \cdot f_{\text{signal}}/f_{\text{clk}})/(\pi \cdot f_{\text{signal}}/f_{\text{clk}})]^2$ , so that if  $f_{\text{clk}}$  is chosen too low the amplifier is ineffective. These considerations lead to the prediction that the efficiency of the amplifier has a broad maximum with respect to  $f_{\text{clk}}$  and the optimal choice is in the vicinity of  $f_{\text{signal}}$ . SPICE simulations using a  $f_{\text{clk}}$  of 2 GHz and power supply voltage  $V_{\text{CC}}$  of 10 V indicate that the efficiency of the example with GaAs HBT's is 85% for full-scale input signal (without accounting for the power needed for the BPDSM or the predriver).

## V. CONCLUSION

A novel amplifier configuration has been proposed and simulated, in which the input signal is passed through a bandpass delta-sigma modulator, a switching mode amplifier, and a tuned output filter. Simulations were shown of a realization of the amplifier using GaAs HBT's. The configuration promises

to offer high efficiency associated with the switching mode amplifier and high linearity associated with the bandpass delta-sigma modulator.

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